The Speed Control of Dual Three Phase Motors Using Nine Switch Z-Source Inverter with SPWM Switching Algorithm

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Abstract: This paper concentrates on "The speed control of dual three phase motors using nine switches Z-source inverter with sinusoidal pulse width modulation switching algorithm". The multi-level inverters are developed to reduce the total third harmonic distortions (THD) in the converters. The multi level converters are used to reduce the switching pattern losses, but THD increases with increasing the levels. This proposed project is minimized the THD with the implementation of z-source voltage source inverter. It is used to boost up the voltage and reduce the voltage fluctuations in the nine-switch z-source inverter. Nine switches - z-source inverter with Sinusoidal PWM techniques are implemented to reduce the switching patterns and get dual 3 phase output voltage which is connected to dual three phase motors like Synchronous motor and Induction motor. The speed control of these motors is based on the v/f control strategy and the switching pattern for that is maintained by PWM technique. The PWM for nine-switch z-source inverter is implemented. In this scheme the sum of modulation indices is equal (or) less than 1.

Keywords: Nine Switch Inverter; Nine Switch Z-Source Inverter; Pulse Width Modulation (PWM).

1. Introduction

Inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries the electrical inverter is a high-power electronic oscillator. It is so named because early mechanical AC to DC converters was made to work in reverse, and thus was "inverted", to convert DC to AC.

It is used mostly in high and medium power industrial applications such as manipulating industrial robots, speed control of electric drives etc.

Generally, the inverter model comprises 6 pulse PWM control for switching the devices and control output voltage for three phase system. Voltage source inverters are used in many high and medium power industrial applications. The CSI has the advantage of indirect output short-circuit protection. In addition, it has a low output harmonic because of its output capacitors. In many industrial applications, there is a need to power two AC loads at the same time .The conventional method of controlling two AC load is to use two separate inverter which have all together 12 switches and the switching patterns involve more THD as well as more cost is required for two separate inverters. Hence, Z-source nine switch inverter is proposed for controlling of two independent AC loads (such as two motors). The input DC voltage of the proposed inverter is shared between two outputs. The Z-source VSI model is designed Z-source VSI with dual 3-phase speed control motors by changing in terms of current switches. The speed is adjustable by varying the SPWM and its controls the output frequency of voltage. Therefore the speed at dual three-phase motor is controlled.

The z-source inverter which has one extra zero vectors to boost up the voltage.

Nine witch converter topology in this the input power is delivered to the output partially through the middle three switches and partially through a quasi DC link circuit. Fourth chapter gives simulation results of VSI. Here the switching pulses is reduced hence the complexity is also reduced. It is used mostly in high and medium power industrial applications.

In this, the nine-switch inverter has three less switches than dual inverter.

2. System Layout

The proposed nine switch Z-source inverter system controls the speed of two independent motors whose overall circuit diagram is depicted in figure below. The system contains a DC source, front end voltage boost up Z-source, nine switch three phase inverter and two independent motors (induction motor and synchronous motor). The switching pulses are generated according to SPWM technique which control the speed of these motors.

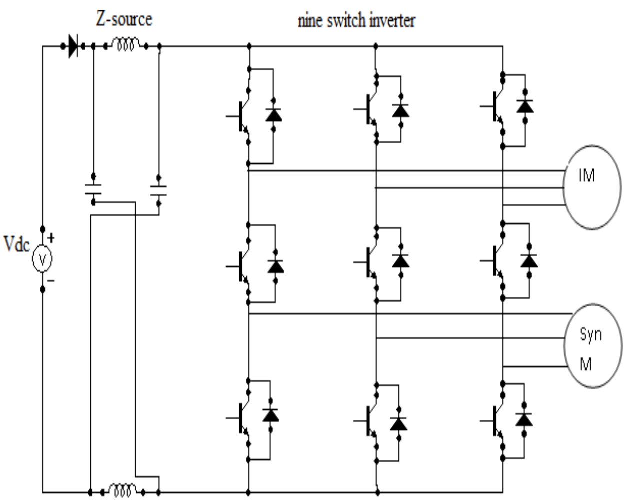

Figure 2.1: Overall layout diagram of proposed nine switch Z-source inverter

2.1 *Carrier-Based PWM Method*

The carrier-based PWM control method for nine-switch inverter is shown in Figure 3. There are two reference signals (upper and lower) for each phase. The upper and lower reference signals are related to upper and lower outputs respectively. The gate signal for upper switch of a leg is generated by comparing the carrier signal and upper reference signal of the related phase (VrefUJ). Similarly, the gate signal for lower switch is generated from the carrier signal and lower reference signal of the related phase (VrefLJ). The gate signal for mid switch is generated by the logical XOR of the gate signals for upper and lower switches. With this method, always two switches are ON in each leg.

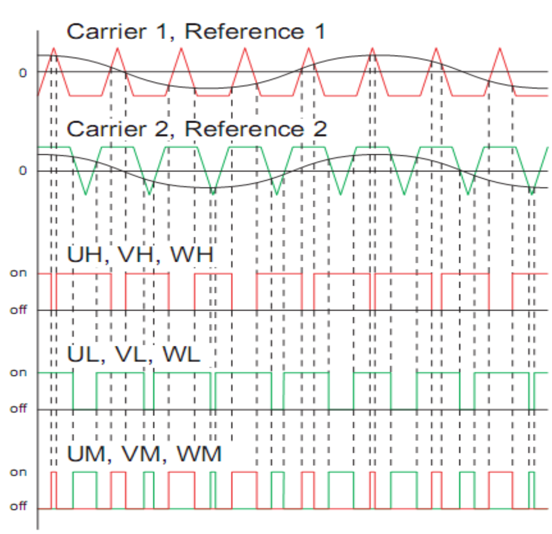

Figure 2.1.1: Carrier-based PWM method for nine-switch inverter

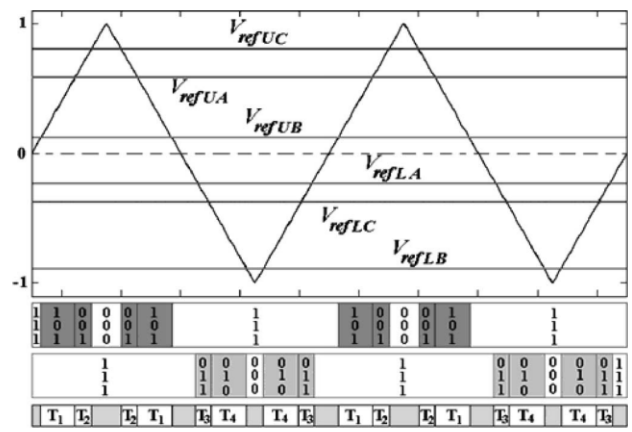

Figure 2.1.2: Carrier-based PWM method switching vector

Figure 2.1.2 shows carrier-based PWM method switching vectors. There are six vectors in each switching cycle for both outputs: two non-zero vectors, one zero vector 0 0 0, two non-zero vectors and one zero vector 1 1 1 {two active—short zero (0 0 0)—two active—long zero (1 1 1)}. In an active vector, output load is connected to the dc input source, while in a zero vector, the output load is short-circuited. When one of the outputs has an active or short zero (0 0 0) vector, the other output has long zero (1 1 1) vector.

Method of Realization

The Carrier1 and the carrier in Figure 2.1.1 can be combined when generating the gate signals. Assume that Vrefu1 and Vrefu2 are given by

$$V_{u1}^{ref} = A_1 \mathrm{Sin}(2\pi f_1 t + \emptyset_1) \quad (1)$$

$$V_{u2}^{ref} = A_2 \mathrm{Sin}(2\pi f_2 t + \emptyset_2) \quad (2)$$

Where A1, A2are amplitudes, f1, and f2 are frequencies, and Φ1, Φ2 are phases. A general modulation rate, m, is given by

$$m = \frac{V^{ref}}{E/2} \quad (3)$$

Where E is a dc source voltage, an offset, E/4, is added to the reference in (1) and an offset -E/4 is added to the reference in (2) when calculating the proposed PWM modulation. Therefore,

$$m_{u1} = \frac{V_{u1}^{ref} + E/4}{E/2} = \frac{V_{u1}^{ref}}{E/2} + \frac{1}{2} \quad (4)$$

$$m_{u2} = \frac{V_{u2}^{ref} - E/4}{E/2} = \frac{V_{u2}^{ref}}{E/2} - \frac{1}{2} \quad (5)$$

From these transformations, the range of the references for Inv1 and Inv2 become $-E/4 \leq V^{ref}_{u1} \leq E/4$ and $-E/4 \leq V^{ref}_{u2} \leq E/4$, respectively. The gate signals for the switches UH, VH, and WH are positive logic values generated by the reference for Inv1 and the upper part of the carrier.

The gate signals for switches UL, VL, and WL are negative logic values generated by the reference of Inv2 and the lower part of the carrier. The gate signals for the switches UM, VM, and WM are generated by the logical XOR value of the gate signals for switches UH, VH, WH and UL, VL, WL, as shown in Fig 2.1.1

2.1.1 Improving the Voltage Utilization

The nine-switch inverter shares one dc voltage source between Inv1 and Inv2. Therefore, voltage utilization for Inv1 and Inv2 is 50%. However, this section proposes a method of improving voltage utilization. Each inverters use of the voltage source changes with its reference value. Let the distribution rate of voltage utilization be α (0≤α≤1). First, we derive an equation for a single phase. α is given by

$$\propto = \frac{A1}{A1+A2} \tag{6}$$

An offset using this is added to the variations of the reference for Inv1 and Inv2.

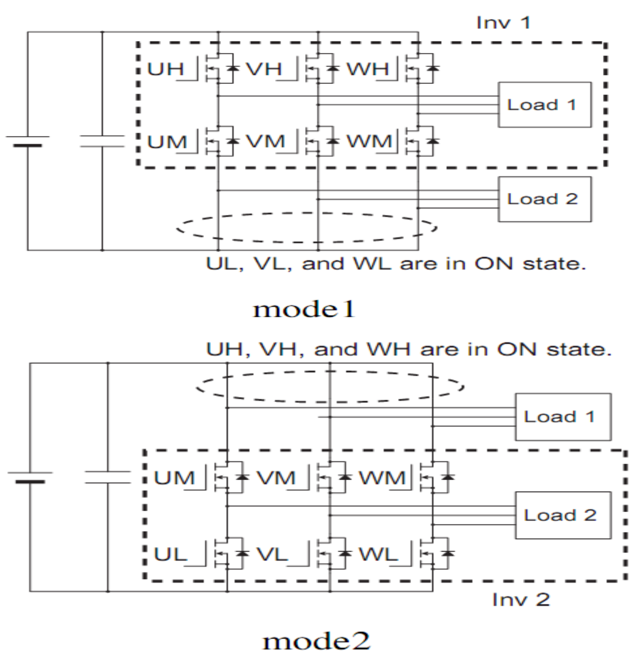

Figure 2.1.2: Operation mode (mode1 and mode2)

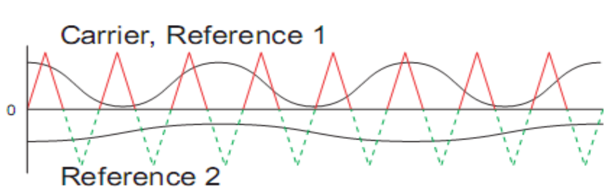

Figure 2.1.3: PWM modulation of the novel inverter

The offsets are decided as modulation rates located on the center of the divided carrier. Thus, each offset is given by

$$\text{offset}_1 = 1-\propto \tag{7}$$

$$\text{offset}_2 = -\propto \tag{8}$$

Therefore, the modulation rate of the U-phase is given by

$$m_{u1} = \frac{V_{u1}^{ref}}{E/2} + 1-\propto \tag{9}$$

$$m_{u2} = \frac{V_{u2}^{ref}}{E/2} -\propto \tag{10}$$

Next, we derive an equation for three-phase operation. The maximal value of each absolute of the three-phase reference is represented by r1and r2.

Finally, the rate of apportionment and the modulation rate are given by

$$\propto = \frac{|r_1|}{|r_1|+|r_2|} \tag{11}$$

$$m_1 = \frac{V_1^{ref}}{E/2} + (1-\propto)e \tag{12}$$

$$m_2 = \frac{V_2^{ref}}{E/2} -\propto e \tag{13}$$

Where,

$$V_i^{ref} = [V_{ui}^{ref} \quad V_{vi}^{ref} \quad V_{wi}^{ref}] \tag{14}$$

$$m_i = [m_{ui}\ m_{vi}\ m_{wi}] \tag{15}$$

$$e = [1 \quad 1 \quad 1]^T \tag{16}$$

$$i = 1,2; -1 \le m_i \le 1$$

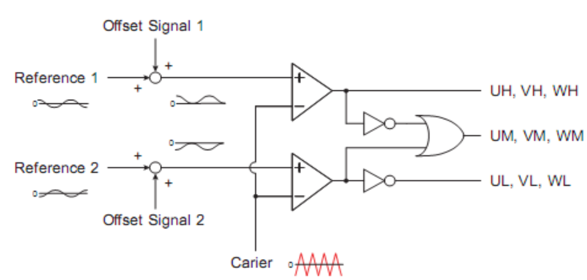

Figure 2.1.4: Method of generation gate signals

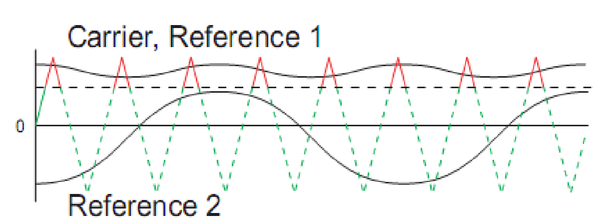

Figure 2.1.5 PWM modulation with the distribution rate of voltage utilization

This method can improve voltage utilization of either Inv1 orInv2. Figure 2.1.5 shows PWM modulation with the distribution rate of voltage utilization.

2.2. *Z-Source Inverter*

The Z-source network was used as front-end boost converter for a conventional inverter .The Z-source inverter is shown in Figure 2.2.1

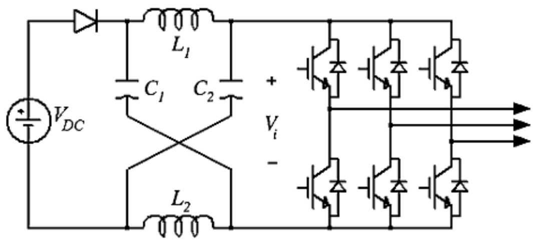

Figure 2.2.1: Voltage type Z-source inverter

In this state, load terminals are shorted through both the upper and lower devices of any one phase leg, any two phase legs, or all three phase legs. The voltage of dc link can be expressed as

$V_i = BV_{dc}$ (1)

Where V_{dc} is the source voltage and B is the boost factor that is determined by

$$B = \frac{1}{1 - 2(\frac{T_0}{T})} \quad (2)$$

Where, T_0 is the shoot-through time interval over a switching cycle T. The output peak phase voltage V_{ac} is

$$V_{ac} = MB\frac{V_{dc}}{2} \quad (3)$$

The capacitors voltage can expressed as

$$V_c = V_{c1} = V_{c2} = \frac{T_1}{T_1 - T_0} V_{dc} \quad (4)$$

Where, $T_1 = T – T_0$ (5)

Relationship between V_i and V_c can be written as

$V_i = 2V_c – V_{dc}$ (6)

And current ripples of inductor can be calculated as

$$\Delta I = \frac{T_1 T_0}{T_1 - T_0}\frac{V_{dc}}{L} \quad (7)$$

Figure lines as shoot-through signals, V_{sc} and $–V_{sc}$.

The value of V_{sc} is calculated by

$$V_{sc} = \frac{T_1}{T} \quad (8)$$

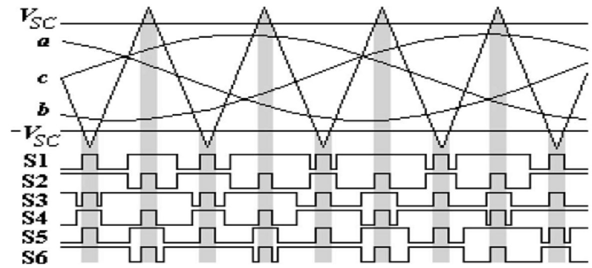

Figure 2.2.2: PWM controls method for Z-source inverter.

2.2.1 *Review of a Z-Source Two-Level Inverter*

Figure 2.2.3 shows the topology of a Z-source two-level voltage type inverter, impedance network that is composed of a split inductor (L_1 and L_2) and two capacitors (C_1 and C_2), which are shown shaded in the figure.

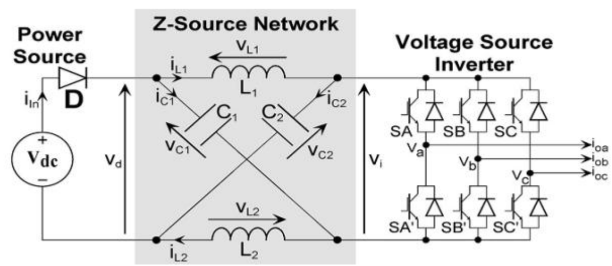

Figure 2.2.3: Topology of a Z-source two-level inverter.

Inductor Design

The voltage across the inductor is the difference between the input voltage and the capacitor voltage. The average current through the inductor is

$$I_L = \frac{P}{V_{in}},$$

Where *P* is the total power and V_{in} is the input voltage. The maximum shoot-through duty cycle can be calculated by

$$\frac{1}{1 - 2D_0} = \frac{400}{250}$$

Or, $D_0 = 0.1875$

For a switching frequency of 10 kHz, the shoot-through time per cycle is 18.75 µs. The capacitor voltage during that condition is

$$V_c = \frac{400+250}{2} = 325V$$

To keep the current ripple less than 120 A, the inductance must be no less than

$$\frac{18.75*325}{132} = 46.2\mu H$$

To minimize the size and weight of the inductors, the two inductors are built together on one core. For a single coil on one core, the flux through the core is

$\varphi = PNi$,

Where P is a constant related to the core material and dimension, N is the number of turns of the coil, and i is the current through the coil. The inductance of the coil is

$$L = \frac{N\varphi}{i} = PN^2$$

For the two inductors in the Z-source inverter, because of the symmetry of the circuit, the current through the inductors is always exactly the same. For two coils on one core with exactly the same current, i, the flux through the core is

$$\varphi = 2PN_i$$

The resulting inductance of each coil when supplying exactly the same current to the two coils is

$$L = \frac{N\varphi}{i} = 2PN^2$$

The inductance of each coil is doubled. Therefore, equivalently, we need to build two coils with 23.1 μH/286 A each on one core; or, say, one coil with 23.1 μH/572 A. A Metglas AMCC_250 core was selected to reduce the loss. Choosing maximum B=1.2 T at peak current,

$$I_{peak} = 440 * 1.3 = 572A$$

$$N = \frac{LI}{BS} = 9.72$$

Where S is the area of the core, which is 11.4 cm2, we take 10 turns.

Capacitor Selection

The purpose of the capacitor is to absorb the current ripple and maintain a fairly constant voltage so as to keep the output voltage sinusoidal. During shoot-through, the capacitor charges the inductors, and the current through the capacitor equals the current through the inductor.

Therefore, the voltage ripple across the capacitor can be roughly calculated by

$$\Delta V_c = \frac{I_{av}\, T_0}{C}$$

Where Iav is the average current through the inductor, T0 is the shoot-through period per switching cycle, and C is the capacitance of the capacitor. To limit the capacitor voltage ripple to 3% at peak power, the required capacitance is

$$C = \frac{200 * 18.75\mu}{325 * 3\%} = 384.6\mu F$$

.

2.3 Motors

In this project we use the two AC motors having individual characteristics i.e. one of them is induction motor where as other is synchronous motor. The Three-phase induction motors are commonly used in adjustable speed drives and they have 3-phase stator and rotor windings. And the three phase synchronous motor is a constant speed machine and rotates with zero slip at the synchronous speed, which depends on number of poles.

The speed controls of both motors are done on the principle of v/f control strategy.

2.4 Speed Control Scheme

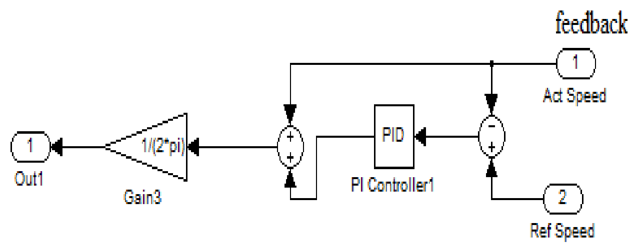

Figure 2.4.1: speed control

The reference speed of both motors are taken in rad/sec and the actual speed (feedback) is also in same unit, then both signal are compared and the error signal is fed to PID controller from where controlled signal of speed is converted to frequency for reference signal of PWM which is modulated with carrier based PWM and the gate pulses for nine switches are generated. In this way the speed control of both motors are controlled.

3. Simulation and Result

While simulation we found that the output voltages of upper (Inv_1) at 50 Hz and that is for lower (Inv_2) at 60 Hz. The two voltage waveform at different frequencies are shown in Figure 3.3. the improvement in voltage due to Z-source is shown is Figure 3.2. the induction and synchronous motor characteristics are shown in Figure 3.4 and Figure 3.5 respectively. The speed controls of both the motors are shown in respective figures.

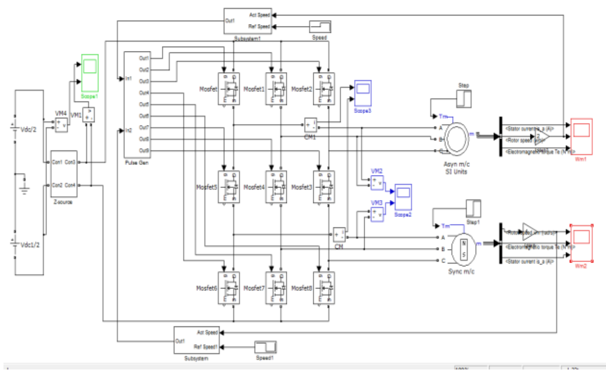

Figure 3.1: Simulation circuit of speed control of dual motors

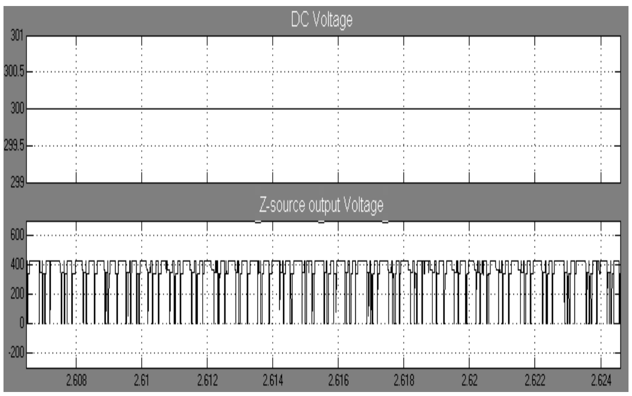

Figure 3.2 (a): DC supply voltage and (b) Z-source output voltage

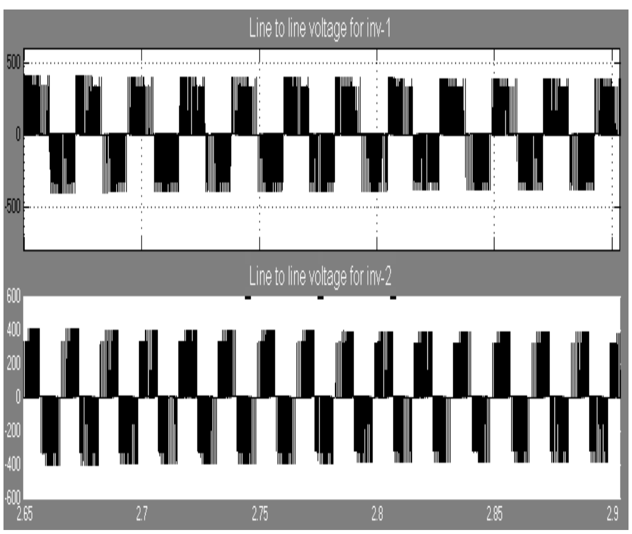

Figure 3.3 (a): Inv_1 voltage and (b) Inv_2 voltage

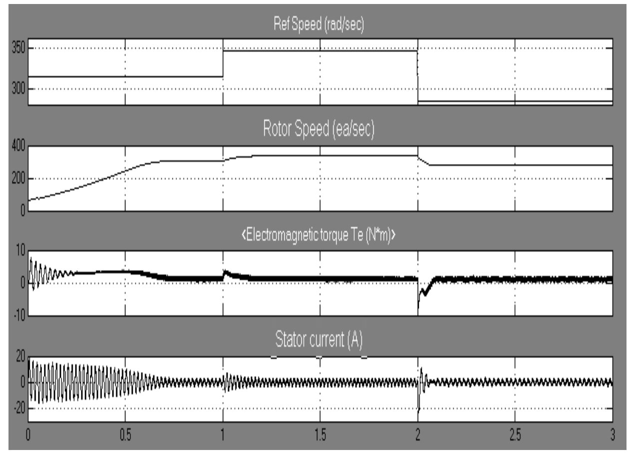

Figure 3.4: Induction motor characteristics

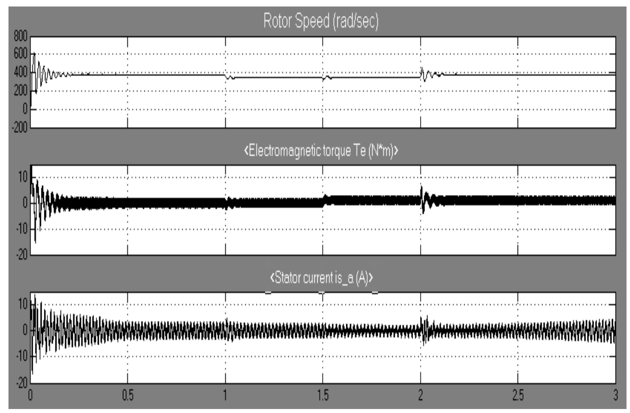

Figure 3.5: Synchronous motor characteristics

4. Conclusion

This paper proposes a *nine-switch Z-source inverter* and a PWM method that can independently control two three-phase loads. The simulations were performed to verify the validity of the proposed inverter. The results confirmed that the *nine-switch inverter* can independently control amplitude and frequency for two three-phase loads, and three phase AC synchronous motors; however, there is some ripple amplitude, and slight interference between *Inv1* and *Inv2*. Work is needed to improve of the interference problem.

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